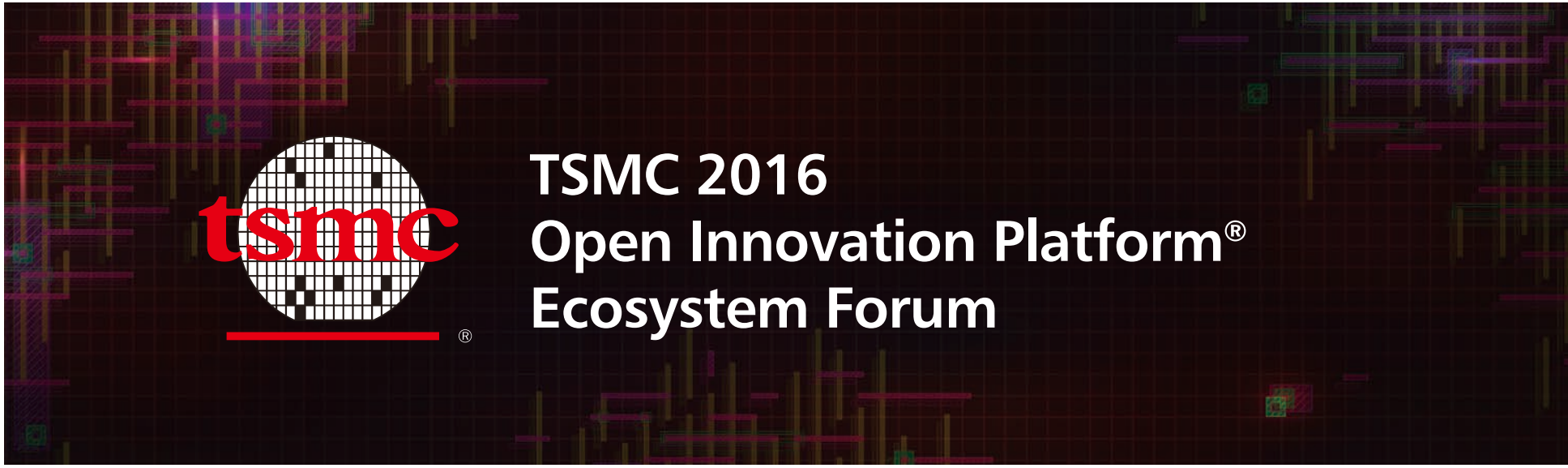
On-chip ESD protection for 16nm FF+

Sofics



ABSTRACT

Despite the rising cost for IC development, EDA tools and mask sets, many fabless design companies continue to use the most advanced CMOS technology because benefits like lower power dissipation, increased gate density, higher speed and lower manufacturing cost per function more than compensate the higher cost.

Due to the use of sensitive elements (such as ultra-thin oxide transistors, FinFET transistors, ultra-shallow junctions, narrow and thin metal layers), increased complexity through multiple voltage domains and the use of IP blocks from various vendors, a comprehensive ESD (Electrostatic Discharge) protection strategy becomes more important at every node.

This presentation shows ESD relevant analysis of 16nm FF+ technology and provides information about state-of-the-art ESD clamps that provide competitive advantage due to ultra-low leakage, reduced silicon footprint and low parasitic capacitance. With the right ESD approach advanced applications (high speed SerDes, IoT, wireless, computing) are within reach.

ON-CHIP ESD PROTECTION FOR 16NM FF+

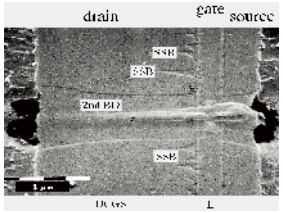
TSMC 2016 NA OIP
Ecosystem Forum
San Jose
Bart Keppens – Sofics

OUTLINE: ESD protection for 16nm FF+

- On-chip ESD protection
- ESD analysis of 16nm FF+
  - Sensitive transistors
  - Metallization constraints
  - Design complexity
- ESD clamp solutions for 16nm
  - Core: 0.8V, 1.2V, 1.5V
  - IO: 1.8V, 2.5V, 3.3V
  - High voltage: 5V

What is ESD? – Importance for IC industry

- Importance of ESD for IC industry
  - Occurance of ESD events
    - Wafer fabrication, testing, dicing
    - Packaging, assembly, testing
    - IC transportation
    - Board level assembly, testing
    - System level assembly, testing
    - Functional use of systems
  - Silicon melting, junction or gate breakdown
  - Industry quotes about ESD failures:
    - "Responsible for 20-30% of IC failures"
    - "25.8% of the products rejected"
    - **"Estimated 8 to 33% of all product losses"**

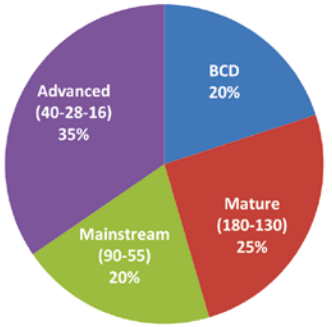


TSMC – Sofics cooperation

- 2008: Design Center Alliance partner
- 2010: IP Alliance partner
- **2016: Sofics serves 40+ TSMC customers**

Open Innovation Platform®

Percentage of projects on TSMC technology nodes



Specialty ESD clamps available on TSMC technology

- Broad solution coverage on TSMC technology
  - Silicon proven solutions, Including different flavours
  - > 250 silicon proven cells – datasheets available online
  - **Portable to other nodes/domains**

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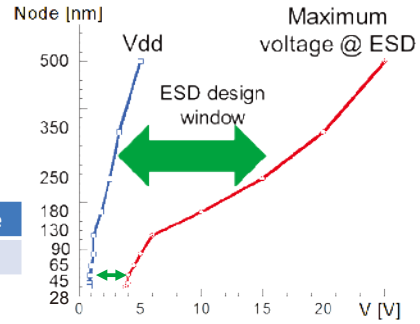
Node	Voltage domains
350nm HV	3.3V 15V
250nm BCD, gen. I and II	12V 24V 40V 60V
180nm BCD, gen. I and II	18V 24V 32V 40V 60V
180nm CMOS	1.8V 3.3V 5V
130nm CMOS	1.0V 1.2V 3.3V 5V 7V
90nm CMOS	1.2V 1.8V 3.3V
65nm CMOS	1.0V 1.2V 1.8V 2.5V 3.3V 5V
40nm CMOS	0.9V 1.2V 1.8V 3.3V 5V
28nm CMOS	0.85V 0.9V 1.8V 3.3V 5V 5.5V 12V
16nm FF+	0.8V 1.2V 1.5V 1.8V 2.5V 3.3V 5V

Problem 1: advanced circuits easily fail during ESD

- Maximum voltage decreases
  - Transient breakdown of gate oxides
  - Burn-out of output drivers
  - Core failure voltage

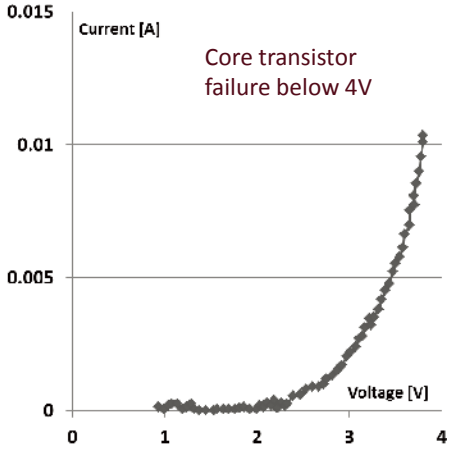


16nm FF+ 0.8V	GOX	Junction	Core
Vmax [V]	3.3	3	3

→ **16nm: Maximum voltage across core transistors 3V**

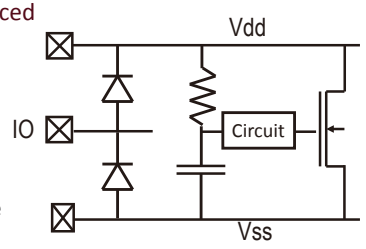
Problem 2a: Traditional solutions run out of steam

- 16nm Core (0.8V) NMOS / PMOS
  - Does not survive snapback
  - **Cannot be used as ESD clamp**
- 16nm IO (1.8V) NMOS/PMOS
  - Does not survive snapback
  - Junction failure at 4.5V
  - **Cannot be used as ESD clamp**
  - **Cannot be made self-protective**



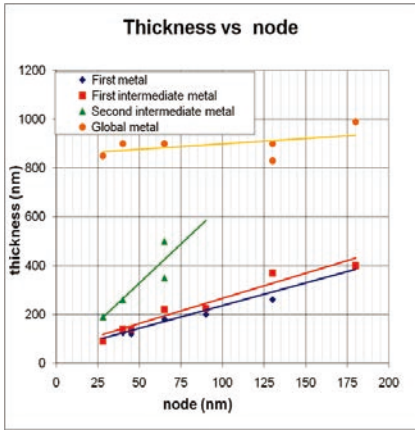
Problem 2b: Traditional solutions run out of steam

- MOS BigFET clamp with enhanced trigger/hold circuit
  - MOS perimeter: 2800um
  - Area is still reasonable: 1800um²
  - **Leakage is the bottle neck: ~0.5uA @ 0.8V @ 85°C**
- ESD performance of diodes further reduced
  - 35mA/um up to 65nm
  - 25mA/um in 40nm
  - 20mA/um in 28nm, 16nm
  - **Diode perimeter scaling required**
    - To compensate for reduced performance
    - Capacitive loading increases



Problem 3: Metallization constraints in adv. CMOS

- 2 groups of metallization
  - Local Metals get thinner (400%)
  - Top metal thickness remains
- Influence on ESD robustness
  - ESD robust power bus still possible
    - Top metal layers remain thick
  - But additional constraints:
    - Connections to the power bus
    - Internal connections inside the ESD clamp



Problem 4: Design complexity increased

- 16nm design complexity
  - Required processing power for verification doubled compared to 28nm
    - Many additional DRC rules
    - Additional verifications for e.g. Multipattern checks
    - Mentor Graphics:
      - "16nm design needs 40-100 CPU cores, 500Gb memory"
  - Design time increased a lot

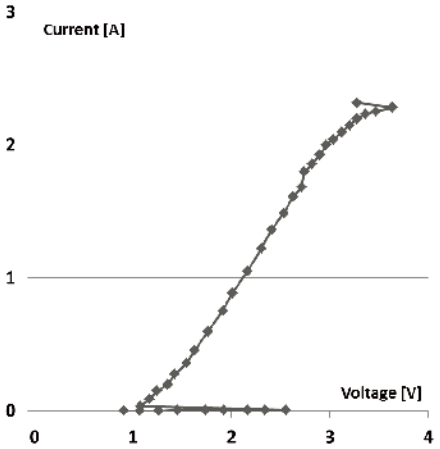
Experienced designer	28nm	16nm
Complete ESD clamp layout with DRC checks	1 day	2 weeks

OUTLINE: ESD protection for 16nm FF+

- On-chip ESD protection
- ESD analysis of 16nm FF+
- **ESD clamp solutions for 16nm**
  - **Core: 0.8V, 1.2V, 1.5V**
  - **IO: 1.8V, 2.5V, 3.3V**
  - **High voltage: 5V**

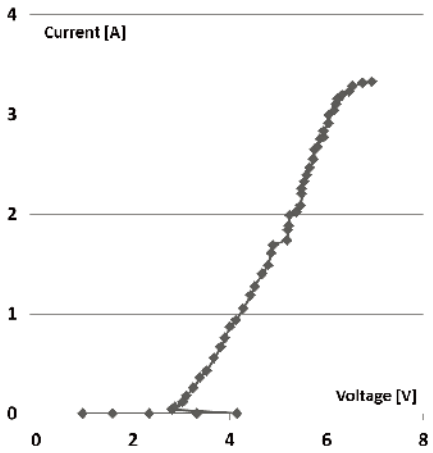
ESD for 16nm FF+ core domain

- Protection of core domain
  - Extremely narrow ESD design window
  - Need efficient power protection clamp
- Best verified solution
  - RC triggered SCR
  - ESD: 1.9A TLP
    - Area: <1000 um²
  - Clamping voltage
    - 0.9V at 125°C
  - Leakage
    - 10nA at 125°C



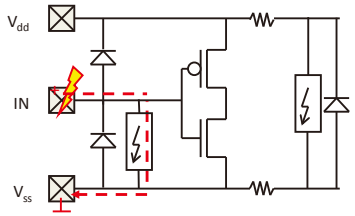
1.8V IO interface protection

- Protection of 1.8V IO interface
  - Protection of GPIO circuits
- Silicon verified solution
  - DT-SCR
  - ESD: 2.0A TLP
    - Area: <1000 um²



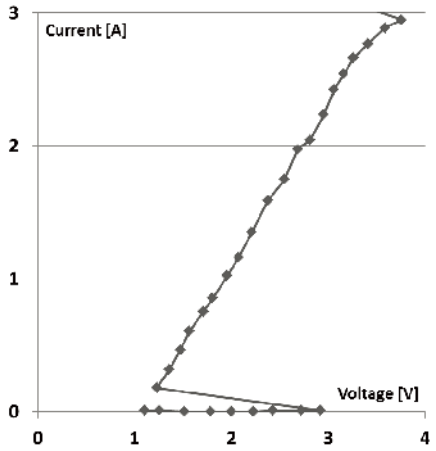
16nm FF+ core interfaces

- Protection of high speed IOs based on core transistors
  - Self-protective devices not possible (does not survive snapback)
  - Dual Diode + railclamp not possible (ESD design window of 3V)
- Solution: Local I/O clamp
  - Strongly reduce voltage drop during ESD
    - Protect extremely sensitive nodes
  - Reduced dependence on bus resistance
  - Optimize for each interface type
  - Allow higher ESD threshold
  - Allow reduced capacitance
  - For wireless or high speed interfaces



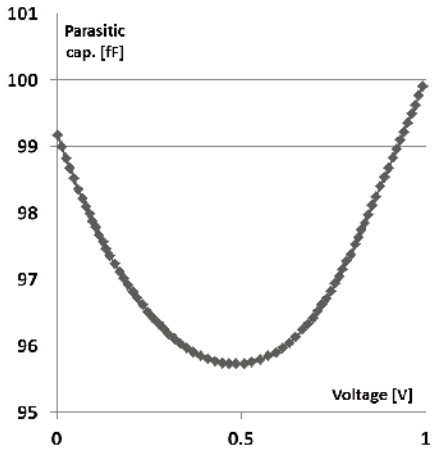
Example 1 for core interface protection

- Protection of core interface
  - Extremely narrow ESD design window
- Silicon verified solution
  - ESD-on-SCR
  - ESD: >2.1A TLP
    - Area: <1000 um²
  - Leakage
    - 1nA at 125°C



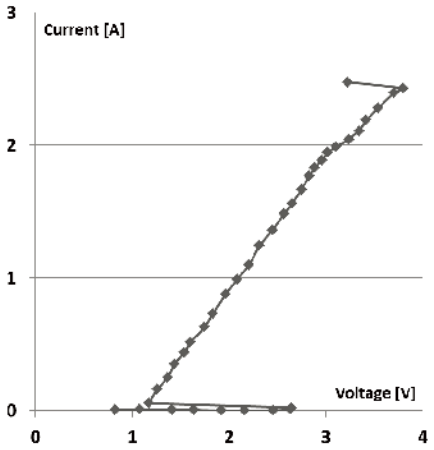
Low parasitic capacitance – high speed interfaces

- Full local protection
  - ESD-on-SCR clamp
  - Protects 0.8V transistors
  - Parasitic junction capacitance
    - ~100fF
  - Suitable for 30Gbps interfaces



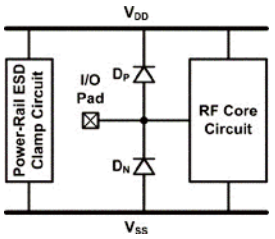
Example 2 for core interface protection

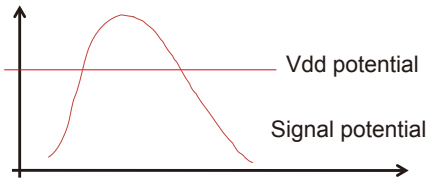
- Protection of core interface
  - Extremely narrow ESD design window
- Silicon verified solution
  - AO-SCR
  - ESD: 2.0A TLP
    - Area: <500 um²



Sometimes a higher voltage tolerance is needed

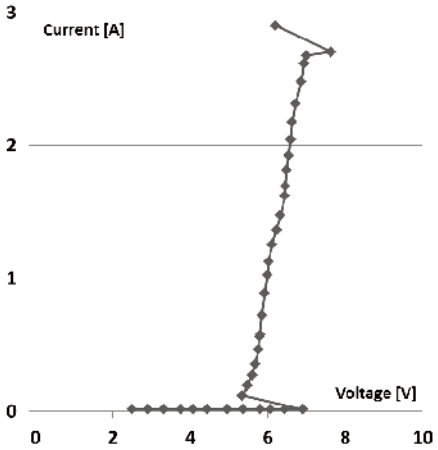
- Traditional ESD solutions can limit the voltage swing on I/O's
  - Higher voltages required for chip-2-chip communications or battery connection
  - Hot swap, fail safe, over voltage tolerant requirements
  - Back drive protection





5V interface protection

- Protection of 5V interface
  - E.g. Li-ion battery connection
- Silicon verified solution
  - N-SMOS
  - ESD: 2.4A TLP
  - Leakage
    - 30nA at 5V, at 25°C
  - Latch-up safe
    - DC Holding voltage > 5.5V



CONCLUSION: ESD protection for 16nm FF+

- ESD protection of 16nm FF+ is not easy
  - Sensitive transistors
  - Increased design complexity
  - Traditional ESD solutions not suitable
- Work with a foundry with a complete IP ecosystem!
- Sofics' ESD clamp solutions
  - Core protection below 3V
  - Several interface protection options
  - Competitive advantage
    - Optimized silicon footprint, capacitance, leakage
    - Possible to protect advanced applications

NOTE